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EXAMINER	
CHAUHAN, ULKA J	
ART UNIT	**PAPER NUMBER**
2676	18

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/815,781	Applicant(s) EBIHARA ET AL.	
	Examiner Ulka J. Chauhan	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-176* is/are pending in the application.

4a) Of the above claim(s) *12-109 and 141-176* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,110-113,117-119,121-133,139 and 140* is/are rejected.

7)☒ Claim(s) *3,6-11,114-116,120 and 134-138* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 12-109 and 141-176 are withdrawn; claims 1-11 and 110-140 are pending.

Election/Restrictions

2. This application contains claims 12-109 and 141-176 drawn to an invention nonelected with traverse in Paper No. 11. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 4, 5, 110-113, 117-119, 121, 128, 129, 131, 132, 139, and 140 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,753,878 to Heirich et al.

5. As per claim 1, Heirich teaches an image generator comprising:

a plurality of graphics processors, each graphics processor being operable to render the image data into frame image data and to store the frame image data and to store the frame image data in a respective local frame buffer (c. 16 ll. 28-40: *one workstation controls the overall image generation process by running a program thread (TH_0), API_0 distributes rendering commands from TH0 among the set of threads TH_1-TH_N running on workstations 1-N. Each thread TH_i relays the rendering commands to an API_i that drives a single graphics accelerator GA_i*; Figs. 1, 4, and 6, and c. 20 ll. 49-56: *The data is sent, as OpenGL commands, over host PCI*

bus 309 to 3D accelerator card 306. 3D rendering chip 310 then executes the OpenGL commands and renders 3D objects to graphics memory 312.);

a control processor operable to provide instructions to the plurality of graphics processors (c. 15 ll. 64-67 and c. 16 ll. 9-10 and Fig. 1: *Image controller 20 passes an object description of the circle to rendering engine 22(1) along with a command to initiate rendering of the circle. Image controller 20 also passes the three other objects to their respective stages for parallel processing.*);

one or more merge units operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce combined frame image data based thereon (Fig. 1: *merge engines 24(1)-24(N)*; c. 12 ll. 49-56: *A distributed synchronization algorithm is implemented in merge engines in order to initiate merging for each image*; c. 6 ll. 1-6: *A data path is provided between each rendering engine 22 and its corresponding merge engine 24 for communicating a part image from the rendering engine to the merge engine, wherein the part image PI_i communicated from rendering engine 22(i) to merge engine 24(i) is a rendered image of the object(s) described by OBJ_i*; c. 6 ll. 30-35: *One of the merge engines 24 is designated as the output merge engine, which is provided with a data path to a frame buffer 26 and holds the output of image generator 12, which is a merged image of all of the part images PI.*); and

means for transmitting the entire combined frame image data to a single display (Fig. 1: *display 16*; c. 16 ll. 61-c. 17 ll. 3: *This image is passed over a private bus to a merge engine (e.g., merge engine 24(i)) and is fed from it into a ServerNet-based pathway of merge engines.*

The final merge engine, 24(N) deposits the fully processed image back into the final frame buffer, or a dedicated frame buffer, from where the image can be sent to a display);

wherein the single display displays the entire combined frame image data on its image area (c. 6 ll. 30-35: *One of the merge engines 24 is designated as the output merge engine, which is provided with a data path to a frame buffer 26 and holds the output of image generator 12, which is a merged image of all of the part images PI*).

6. As per claim 2, Heirich discloses:

at least one of the one or more merge units is operable to produce a merge synchronization signal used by the graphics processors to release the frame image data from the respective local frame buffers to the one or more merge units (c. 12 ll. 49-56: *A distributed synchronization algorithm is implemented in merge engines in order to initiate merging for each image. The following simple process is used in one embodiment by each merge engine MEi: If (MEi+1 asserts "ready" and frame buffer FBi has data) then If (i>1) then [assert "ready"] else [start the data flowing into the pipeline]*).

7. As per claims 4 and 5, Heirich discloses:

the merge synchronization signal is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed

the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed (c. 7 ll. 56-64: *For NTSC television video, the typical format is 30 frames/second with each frame comprising 640 pixels by 480 pixels, for a total of 307,200 pixels per frame. Thus NTSC rendering engines would output between 44 and 70 MBS*

of data ... the HDTV format, with its approximately 2000x1000 pixel frames, requiring a bandwidth of between 286 and 455 megabytes/second).

8. Claims 110-113 are similar in scope to claims 1, 2, 4, and 5, and are rejected under the same rationale.

9. As per claim 117, Heirich discloses:

wherein the image data are rendered into the respective frame buffers asynchronously with respect to the merge synchronization signal (c. 12 ll. 43-47: *Note that rendering can still overlap merging, since the frame buffers are typically double-buffered and the graphics accelerator can start work on the next image while the merge engines are working on the current image*).

10. As per claim 118, Heirich discloses:

wherein the graphics processors can operate in one or more modes that affect at least one of ... and (ii) how the frame image data are merged to synchronously produce the combined frame image data (c. 11 ll. 1-4: *Core 110 will perform different computations in different operating modes*).

11. As per claim 119,

instructing the graphics processors to operate in the one or more modes on a frame-by-frame basis (c. 12 ll. 1-3: *If the merge engine is created using FPGA's as described above, the operations performed by the merge engine can be updated as needed by reprogramming the FPGA's*).

12. As per claim 121, Heirich discloses:

wherein the modes include at least one of area division, averaging: layer blending, Z-sorting and layer blending, and flip animation (c. 10 ll. 48-55: *at least two computations should be supported: a Z comparison operation... and a blend operation...other operations can easily be added to support commercially important markets, including image compositing and digital special effects*).

13. As per claim 125, Heirich discloses averaging mode providing that the local frame buffers of at least two of the graphics processors include rendering areas that each correspond with all portions of the image area and that the respective frame image data from the at least two local frame buffers are averaged to produce the combined frame image data (c. 10 ll. 53-55: *other pixel operations can easily be added to support commercially important markets, including image compositing and digital special effects*; c. 18 ll. 43-47: *virtue of the image composition approach described herein to achieving scalability, in contrast to other architectures, is that there is no subdivision of the image at any point in the architecture*).

14. As per claim 127, Heirich discloses synchronously averaging the frame image data from the respective rendering areas of the at least two graphics processors based on alpha blending values to produce the combined frame image data, and the combined frame image data are capable of covering the image area (c. 11 ll. 13-18: *Instead of computing a pixel color from a single polygon, a rendering system can treat polygons as semitransparent objects and compute pixel colors by blending the colors of a number of polygons along a single line of sight*).

15. As per claims 128 and 129, Heirich discloses:

wherein at least one of the modes is a layer blending mode providing that: (i) at least some of the image data are rendered into the local frame buffers of at least two of the graphics

processors such that each of these local frame buffers includes frame image data representing a portion of the combined frame image data; (ii) each of the portions of the combined frame image data are prioritized; and (iii) the method further comprises synchronously producing the combined frame image data by layering each of the frame image data in an order according to the priority thereof (Fig. 3; c. 16 ll. 17-27: *Along with the pixel values, rendering engines 22 preferably also output Z values for the pixels, where a Z value for a pixel indicates the depth of the portion of object represented by that pixel. Merge engines 24 use the Z values to determine when one object obscures another. For the purposes of illustration, each of the objects are placed at constant depths, with objects* OBJ_1 *-*OBJ_4 *being at depths of 1, 3, 2 and 4, respectively. Here, a lower Z represents a depth further from the view point. This is reflected in the fact that in the final image,* OBJ_1 *(the circle at z=1) is obscured by* OBJ_2 *(the rectangle at x=3) and* OBJ_3 *(the rectangle at x=2)*).

16. Claims 131 and 132 are similar in scope to claims 128 and 129 and are rejected under the same rationale.

17. As per claims 139 and 140, Heirich discloses receiving and storing common image data in a memory; transmitting at least some of the common image data to at least some of the plurality of graphics processors such that (i) at least one of the successive frames of frame image data from one or more of the graphics processors may include at least some of the common image data; and producing a successive frame of the combined frame image data based on the common image data (c. 15 ll. 64-c. 16 ll. 8: *Image controller 20 passes an object description to rendering engine 22 including a texture or a description of the reflectancetransmission*

properties assigned to the object and a description of the light sources or shadows impinging on the object).

18.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

21. Claims 122-124, 126, 130, and 133 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,753,878 to Heirich et al and U.S. Patent No. 6,664,968 to Ono.

22. As per claim 122, Heirich does not expressly teach an area division mode providing that at least two of the local frame buffers are partitioned into respective rendering areas that correspond with respective portions of the image area and non-rendering areas, and an aggregate of the rendering areas results in a total rendering area that corresponds with all portions of the

image area. Ono discloses that a display area of a screen is divided into a plurality of sub-screens and graphics adapters are provided for the respective sub-screens [c. 3 ll. 11-15 and Fig. 1]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the division of the display area of a screen into a plurality of sub-screens as taught by Ono in combination with the image generator and plurality of rendering engines of Heirich's invention in order to provide a higher resolution display.

23. As per claims 123, 126, 130, 133 Heirich does not expressly teach at least two graphics processors complete rendering the image data into the respective rendering areas of the frame buffers prior to the end of each blanking period. Ono discloses that after the vertical retraces corresponding to the two frame buffers 13a and 14a are performed, the switching of one frame buffer, from which image data has been read out to be displayed, to the other frame buffer, from which image data is to be newly read out to be displayed, is performed (c. 9 ll. 66-c. 10 ll. 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the rendering engines of Heirich's invention to complete rendering prior to the end of each blanking period so that proper switching between the display and update buffers of the frame buffers can be carried out as taught by Ono.

24. As per claim 124, Heirich discloses synchronously aggregating the frame image data from the respective rendering areas of the at least two graphics processors based on alpha blending values to produce the combined frame image data, and the combined frame image data are capable of covering the image area (c. 6 ll. 1-6: *A data path is provided between each rendering engine 22 and its corresponding merge engine 24 for communicating a part image from the rendering engine to the merge engine, wherein the part image PI_i communicated from*

rendering engine 22(i) to merge engine 24(i) is a rendered image of the object(s) described by OBJ_i; c. 6 ll. 30-35: *One of the merge engines 24 is designated as the output merge engine, which is provided with a data path to a frame buffer 26 and holds the output of image generator 12, which is a merged image of all of the part images PI*; c. 11 ll. 13-18: *Instead of computing a pixel color from a single polygon, a rendering system can treat polygons as semitransparent objects and compute pixel colors by blending the colors of a number of polygons along a single line of sight*).

Allowable Subject Matter

25. Claims 3, 6-11, 114-116, 120, and 134-138 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

26. Applicant's arguments, see pg. 30, filed 4/28/04, with respect to the rejection(s)of claim(s) 1-11 and 110-140 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Heirich.

Conclusion

27. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5546530 U.S. Patent No. 6157393 U.S. Patent No. 6157395

U.S. Patent No. 6292200 U.S. Patent No. 6329996 U.S. Patent No. 6473086

A. Heirich and L. Moll. Scalable Distributed Visualization Using Off-the-Shelf Components. In *Proceedings of the 1999 IEEE Symposium on Parallel Visualization and Graphics*, pages 55-60, October 1999.

S. Molnar, J. Eyles, and J. Poulton. PixelFlow: High-Speed Rendering Using Image Composition. In *Proceedings of the 19th Annual Conference on Computer Graphics and Interactive Techniques*, vol. 26 issue 2, pages 231-240, July 1992.

S. Nishimura and T. Kunii. VC-1: A Scalable Graphics Computer with Virtual Local Frame buffers. In *Proceedings of the 23rd Annual Conference on Computer Graphics and Interactive Techniques*, pages 365-373, August 1996.

B. Wei, D. Clark, E. Felten, K. Li, and G. Stoll. Performance Issues of a Distributed Frame Buffer on a Multicomputer. In *Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics Hardware*, pages 87-96, August 1998.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is (703) 305-9651. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.
29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (703) 308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
September 6, 2004